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# METHOD AND APPARATUS TO BALANCE REFERENCE SETTLING IN SWITCHED-CAPACITOR PIPELINED DIGITAL TO ANALOG CONVERTER

## RELATED APPLICATION

This application claims the benefit of U.S. Provisional Patent Application No. 60/464,387, filed April 18, 2003. The entire teachings of the above application are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

As progress in Digital-to-Analog Converter (DACs) technology continues to yield devices capable of operating at greater and greater conversion rates, they are capable of supporting an increasing number of applications. For example, very high-speed DACs enable digital processing in applications that had once been limited to the analog domain. Such applications include wired and wireless communication systems. These new applications often demand greater control of harmonic distortion and limitations in power consumption.

One emerging DAC architecture is a pipeline, switched-capacitor DAC as described in "A Quasi-Passive CMOS Pipeline D/A Converter," by F. J. Wang, G. C. Temes, S. Law, published in the IEEE Int. J. of Solid-State Circuits, vol. 24, no. 6, Dec. 1989. An attractive characteristic of this architecture is that it intrinsically does not suffer from major output glitches. On the other hand, current implementations are affected by a number of circuit shortcomings that limit the practically achievable dynamic linearity.

A conventional switched-capacitor pipeline DAC is composed by a cascade of a number of substantially identical cells that cooperatively synthesize an analog representation of a digital quantity by a charge-sharing algorithm driven by input digital data. Each cell is uniquely associated to a respective bit of the digital input and includes, among other components, a capacitor. The capacitor is used to store an intermediate result of the data conversion and further as a processing element for the conversion algorithm. In more detail, each capacitor in the pipeline of cells is pre-charged to one of two different reference voltage levels depending on the logic state of the bit associated with the cell. This type of switched-capacitor DAC is discussed in more detail below.

At least one problem with this approach relates to the settling behavior of the capacitors' pre-charge process depending on the digital code to be converted. Thus, the settling behavior for a cell associated with a logical "1" input will be different than the settling behavior of the same cell associated with a logical "0." Unfortunately, this code dependence results in a degradation of the linearity of the DAC. Further complicating matters, the source circuit providing the reference voltage levels is also disturbed by the pre-charge process. This disturbance too is code-dependent.

## SUMMARY OF THE INVENTION

The present invention solves the problems of the prior art switched-capacitor DACs by providing a cost-effective and efficient architecture and process that significantly reduce code-dependency on the pre-charge process and on the reference settling behavior.

In one aspect, the invention relates to a switched-capacitor digital-to-analog converter (DAC) including a number of cells, with each cell including first and second switches. The first and second switches switch respective voltages from a source to a charged capacitor. The DAC includes respective switch driver circuits, each in electrical communication with a respective one of the first and second switches. Each of the switch driver circuits applies a switch control signal to a respective one of the first and second switches. The switch control signals that turn the switch on differ to equalize the gate-to-source voltage difference.

The first and second switches can be transistor switches, such as metal-oxide-semiconductor (MOS) devices. Thus, the switch control signal can be a gate voltage controlling a MOS transistor between switching states.

In some embodiments, the respective switch driver circuits each include a first element receiving an external input, the first element providing an output responsive to the received input. The respective switch driver circuits each also include second element in electrical communication with the first element. The second element receives the output and conditions the output according to the difference between the respective voltages from the source.

The first element can be a logic gate, such as a NAND gate, receiving one bit of a digital input word and a switching control signal. The switching control signal, in turn, can be a clock signal. Additionally, the second element can also be a logic device, such as an inverter, powered by a logic source level depending on the difference between the respective voltages from the source.

Still further, the source can include two emitter follower circuits and a resistor network, each coupled between electrical power and ground. The emitter follower circuits can include bipolar junction transistor devices.

In another aspect, the invention relates to a process for data conversion using a switched-capacitor DAC including the steps of providing a plurality of cells, including first and second switches. The switches switch respective different voltages from a source to a charged capacitor. The process also includes providing respective switch driver circuits each in electrical communication with a respective one of the first and second switches. The switch driver circuits apply respective switch control signals to respective ones of the first and second switches. In particular, the switch control signals that turn the switch on are different to equalize the gate-to-source voltage difference.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters

refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIG. 1A is a schematic diagram of one embodiment of a switched-capacitor Digital-to-Analog Converter (DAC);

FIG. 1B is a more detailed schematic diagram of one embodiment of a representative cell of the switched-capacitor DAC of FIG. 1A;

FIG. 1C is a more detailed schematic diagram of an alternative embodiment of a representative cell of the switched-capacitor DAC of FIG. 1A;

FIG. 1D is a more detailed schematic diagram of the source interconnection to a representative cell of the switched-capacitor DAC of FIG. 1A;

FIG. 2A is a more detailed schematic diagram of one embodiment of a compensating switch driver used in a representative cell of the switched-capacitor DAC of FIG. 1A;

FIG. 2B is a more detailed schematic diagram of an alternative embodiment of a compensating switch driver used in a representative cell of the switched-capacitor DAC of FIG. 1A;

FIG. 3A is a schematic diagram of one embodiment of a transistor-based source-interconnect circuit;

FIG. 3B is a schematic diagram of an alternative embodiment of a transistor-based source-interconnect circuit;

FIG. 4A is a schematic diagram of one embodiment of a buffer-based source-interconnect circuit; and

FIG. 4B is a schematic diagram of an alternative embodiment of a buffer-based source-interconnect circuit.

## DETAILED DESCRIPTION OF THE INVENTION

A description of preferred embodiments of the invention follows.

Disclosed herein is a method and apparatus to improve the linearity of pipelined switched-capacitor digital to analog converters by balancing the settling behavior of its pre-charge switches. In more detail, a switched capacitor DAC includes a number of substantially identical cells, one cell for each bit of an input digital word. A number of

switch driver circuits are used to apply respective switch control signals to turn respective switches on and off. Advantageously, the switch control signals differ by an amount determined to equalize the gate-to-source voltage difference between different switches.

One embodiment of a switched capacitor DAC is shown in FIG. 1A [2]. A 3-phase clock $\{\phi_1\ \phi_2\ \phi_3\}$ sets the basic timing for the DAC operation, which is described in detail in references [1] and [2] cited at the end of this document.

In the following it is assumed that the digital input of the DAC is represented by a set of N bits $\{b_0\ b_1\ b_2\ \ldots\ b_{N-1}\}$, where $b_0$ represents the least significant bit (LSB), while $b_{N-1}$ represents the most significant bit (MSB). Finally, let be $Vref_1$ and $Vref_2$ two reference (DC) voltage levels.

In the following, we will assume that the power supply voltage of all the logic gates is $V_{dd}$ unless differently specified.

As shown in FIG. 1A, the SC pipeline DAC is essentially composed of a cascade of identical cells. One for each bit $b_k$. One of these (for example $b_1$) is shown in FIG. 1B where the switches have been implemented with actual MOSFET devices. Here, the series combination of the sampling switch controlled by $\phi_1$ and the two-way switch controlled by $b_1$ has been implemented using two single MOSFET switches M2 and M3 controlled by proper logic combinations of $b_1$ and $\phi_1$ as proposed in [2-3]. A pseudo-differential implementation of this unity cell is shown in FIG. 1C.

Let us first concentrate on the single-ended implementation of FIG. 1B for simplicity. On $\phi_1$ the capacitor C is connected to one of the two reference voltages $Vref_1$ or $Vref_2$ depending on the logic state of $b_1$. Specifically, M2 will be turned on (and M3 will be turned off) if $b_1=1$; conversely, M3 will be turned on (and M2 will be turned off) if $b_1=0$.

It is important, at this point, to observe that the time-constant for the settling of the voltage across the capacitor C toward its steady-state value $Vref_1$ or $Vref_2$ will depend on $b_1$. To understand this, it will just suffice to notice that the on-resistance of the switches M2 and M3 are inversely proportional to the voltage differences $(VG2-Vref_1)$ and $(VG3-Vref_2)$ respectively; VG2 (respectively VG3) will be equal to the power supply voltage $V_{dd}$ if $b_1=1$ (respectively $b_1=0$) and equal to the ground voltage if $b_1=0$

(respectively $b_1$=1). A similar observation can be made for the pseudo-differential implementation shown in FIG. 1C.

It may be worth noticing that, if we assume $Vref_1$>$Vref_2$, then the on-resistance of M3 will be smaller than the on-resistance of M2. Consequently, M2 will determine the slowest settling and, hence, limit the speed at which the pre-charge can be accomplished. Incomplete settling will introduce a code-dependent error, hence harmonic distortion on the DAC's output.

Moreover, when M2 (respectively M3) is switched-off, right after the pre-charge to $Vref_1$ (respectively $Vref_2$) is completed, a charge which is function of $V_{dd}$-$Vref_1$ (respectively $V_{dd}$-$Vref_2$) will be injected by this MOSFET into C. The charge injected depends on the logic state of $b_1$ as it is function of (VG2-$Vref_1$) and (VG3-$Vref_2$) as well.

In an actual circuit, the difference in settling behavior will not only be limited to the different time constant, as just explained. Actually, the entire behavior of the settling will be affected. Let us consider the circuit shown in FIG. 1D. Here a model of a real reference circuit has been added to the cell of FIG. 1A. Specifically, $Vref_1$ (respectively $Vref_2$) is generated by the reference model composed by $V_{R1}$ and $Z_{S1}$ (respectively $V_{R2}$ and $Z_{S2}$). Such a reference is often provided by a circuit which can be external to the chip integrating the DAC. Alternatively, the reference circuit could be integrated on the same die containing the DAC, but it may need to be connected to the DAC through an off-chip connection to allow for external capacitive decoupling. In either of these cases, the actual connection between the references and the DAC's cells will encounter a non-negligible parasitic inductance, here modeled by the two inductors $L_1$ and $L_2$ respectively.

The circuit composed by $V_{R1}$, $Z_{S1}$, $L_1$, M2 and C (respectively $V_{R2}$, $Z_{S2}$, $L_2$, M3 and C) constitutes a well-known RLC network which can have very different settling behavior depending on the values of its components. A reasonable package design will try to make $L_1$=$L_2$. However, as we have seen before, the on-resistance of M2 and M3 will differ. Hence, the damping of $V_{ref1}$ and $V_{ref2}$ will always be different.

It could be, in principle, conceivable to compensate this difference by properly setting the references' source impedances $Z_{S1}$ and $Z_{S2}$ (for example, by setting $Z_{S1}$ to the on-resistance of M3 and by setting by setting $Z_{S2}$ to the on-resistance of M2). But this wouldn't be very practical to accurately realize. Moreover it would double the total

series resistance of the pre-charge circuit, hence it would significantly degrade the speed of the DAC.

In conclusion, because of the intrinsic code-dependence of the on-resistance of the pre-charge switches, the corresponding settling is affected and can result into harmonic distortion of the digital to analog conversion.

Moreover, because of the different steady-state value of the gate-source voltages of the same pre-charge switches, the charge injected on to the capacitors once the switches open, will depend to the code as well. Ideally, this last effect should only result in gain error instead of harmonic distortion (as described in [1-2]). In reality, because of actual mismatches between the cells composing the array, this will introduce different gain errors for different cells and hence will contribute to harmonic distortion and code-dependency as each cell corresponds to a different bit.

An apparatus that significantly improve the above-mentioned problems is shown in FIG. 2A in its single-ended form. This circuit differs from the one shown in FIG. 1B as the AND gates A1 and A2 have been replaced by the NAND gates N1 and N2 and by the inverters I1 and I2. The power supplies of these two latter inverters are connected to the voltages $V_{GR1}$ and $V_{GR2}$ respectively instead of $V_{dd}$. Because of this, the output voltage of I1 (respectively I2) will be equal to $V_{GR1}$ (respectively $V_{GR2}$) when its input is a logic zero; conversely, it will be equal to the ground voltage when its input is a logic one.

$V_{GR1}$ and $V_{GR2}$ are chosen such that $V_{GR1} - Vref_1 = V_{GR2} - Vref_2$. By doing so, the on-resistance of M2 and M3 is now independent from $Vref_1$ and $Vref_2$ and, consequently, it is independent from the logic state of $b_1$. A number of possible ways to make $V_{GR1} - Vref_1 = V_{GR2} - Vref_2$ will be discussed in the following.

Then, when this condition is satisfied, all the issues mentioned in the previous Section are solved. The settling behavior of M2 and M3 is the same and it does not depend on the state of $b_1$ anymore. Because of that, to a first order, incomplete settling behavior is not code-dependent anymore and does not introduce harmonic distortion.

Therefore it is possible to reduce the size of the switches M2 and M3, with several additional benefits to the performance of the DAC, such as:

- Smaller charge injection from M2 and M3; this directly improves the linearity of the DAC;
- Smaller parasitic capacitors; in particular, smaller drain-bulk and source-bulk junction (nonlinear) capacitors; this directly improves the linearity of the DAC
- It is then possible to accordingly reduce the size of the inverters I1 and I2 (and, possibly, N1 and N2) with advantage in terms of reduction in area and power consumption;

Furthermore, the charge injected into C when either M2 or M3 turn off, is now code-independent as well.

In reality, the dependence from $Vref_1$ and $Vref_2$ (and, hence, from the digital input $b_1$) may not be entirely removed as the threshold voltages of M2 and M3 depend on their bulk-source voltages $V_{bs2}$ and $V_{bs3}$. If the technology used to integrate the DAC allows to short-circuit the bulk and source terminals of both M2 and M3, then $V_{bs2} = V_{bs3} = 0$ and the code-dependence is entirely removed. This is possible if the technology allows making separate wells for M2 and M3.

Conversely, if that is not allowed and the bulk terminals are connected to ground, then $V_{bs2}=Vref_1$ and $V_{bs3}=Vref_2$. In this latter case, there will still be some residual code-dependence through the well-known "bulk-effect". However, the invention will still provides a considerable improvement over the prior art as the major contribution to the code-dependence has been cancelled.

A pseudo-differential version of the implementation of FIG. 2A has been shown in FIG. 2B. It will be apparent to those skilled in the art that another version of the circuits of FIG. 2A and 2B using PMOS switches (or CMOS transmission gates) in place of the NMOS switches can be easily proposed without departing from the spirit of this invention.

In a further modification to the preferred embodiment, if $Vref_1>Vref_2$ then we can set $V_{GR1} = V_{dd}$ and $V_{GR2} = V_{dd} - Vref_1 + Vref_2$. This choice satisfies the above condition $V_{GR1} - Vref_1 = V_{GR2} - Vref_2$ and offers two main advantages:

- The settling time for the pre-charge process is the fastest possible; and
- The implementation of the source for $V_{GR1}$ is trivial as it is possible to use directly the power supply $V_{dd}$ itself.

Those skilled in the art will recognize that the implementation of the voltage sources for $V_{GR1}$ and $V_{GR2}$ can be obtained in several different ways. One possible example will be provided here.

The circuits shown FIGS. 3A and 3B respectively represent embodiments of the reference voltage generators $Vref_1$ and $Vref_2$ and the voltage sources $V_{GR1}$ and $V_{GR2}$.

In fact, assuming that the base currents of the bipolar transistors of both circuits are negligible with respect to $V_{dd}/(R_1+R_2+R_3)$, it can be easily proved that $V_{GR1}$ and $V_{GR2}$ satisfy the required condition $V_{GR1} - Vref_1 = V_{GR2} - Vref_2$.

The circuits shown FIGS. 4A and 4B respectively represent alternative embodiments of the reference voltage generators $Vref_1$ and $Vref_2$ and the voltage sources $V_{GR1}$ and $V_{GR2}$.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

REFERENCES:

[1] F. J. Wang, G. C. Temes, S. Law, "A quasi-passive CMOS pipeline D/A converter," IEEE Int. J. of Solid-State Circuits, vol. 24, no. 6, Dec. 1989.

[2] K. Khanoyan et al., "A 10b, 400 MS/s glitch-free CMOS D/A converter," Proc. of IEEE 1999 Symp. on VLSI Circuits, pp. 73-76, 1999.

[3] A. Rofougaran et al., "A single-chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-$\mu$m CMOS—Part I: Architecture and Transmitter Design," IEEE Int. J. of Solid-State Circuits, vol. 33, no. 4, Apr. 1998.